AMENDMENTS TO THE CLAIMS

Please change the claims as follow:

1. (Currently Amended) A data transfer circuit for latching an input data in a first latch section, transferring ~~data of~~ a first latch result of said first latch section to a second latch section, and latching said first latch result ~~therein~~in said second latch section, characterized by:

transferring ~~data of~~ only an inverted output of ~~the~~ said first latch result ~~of said first latch section~~ to said second latch section or transferring only a non-inverted output of said first latch result to said second latch section; and

~~at least during a period of data transfer of the latch result of said first latch section to said second latch section, causing~~ raising a power supply voltage of said first latch section from a first voltage to a second voltage ~~to rise~~ while said first latch result is transferred to said second latch section;

wherein said second voltage is higher than said first voltage, and

wherein said second voltage is a power supply voltage of said second latching section.

2. (Withdrawn) A flat display apparatus that sequentially inputs gradation data indicative of brightness of each pixel and displays an image based on said gradation data in a predetermined display section, said flat display apparatus characterized by having:

a plurality of latch circuits for sampling said gradation data sequentially and cyclically, and distributing said gradation data to a corresponding line; and

a digital/analog conversion circuit for setting an output signal level to said corresponding line depending on a latch result of said latch circuits, in which each of said plurality of latch circuits is characterized by:

latching said gradation data in a first latch section at a respective timing corresponding thereto, data transferring a latch result of said first latch section to a second latch section simultaneously and in parallel in said plurality of latch circuits to output the result to said digital/analog conversion circuit;

data transferring only an inverted output of the latch result of said first latch section or only a non-inverted output of the latch result of said first latch section to said second latch section; and

raising a power supply voltage of said first latch section at least during a period of data transfer of the latch result of said first latch section to said second latch section.

3. (New) The data transfer circuit according to claim 1, wherein said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to a transfer of said first latch to said second latch section by only an inverted output or only a non-inverted output.